

# High Performance Computing

## Roofline

### Project 3

Johannes Winklehner

Armin Friedl

1226104

1053597

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A *roofline model* for a multicore-processor is obtained by calculating the theoretical peak performance of the processor and benchmarking the peak memory bandwidth. Two artificial computational kernels with arithmetic intensities of  $\frac{1}{16}$  GFLOPs/Byte and 8 GFLOPs/Byte are devised. The performance of the two kernels is then compared to the theoretical calculations in the roofline model.

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# 1 Introduction

## 2 Roofline Model

### 2.1 Theoretical Peak Performance

The CPU under test was a Intel® Core™ i5-4210U. Table 1 shows the relevant specifications for this processor according to Intel Ark [3].

Specification	Value
Instruction Set Extension	SSE4.1/4.2, AVX 2.0
# of Cores	2
Processor Base Frequency	1.7 GHz
Max Turbo Frequency	2.7 GHz
Microarchitecture	Haswell

Table 1: Intel® Core™ i5-4210U processor specifications [3]

The 4th generation Intel Core processors provide FMA<sup>1</sup> and AVX<sup>2</sup> extensions [2, 5-2 Vol.1]. An FMA unit is capable of “[...] 256-bit floating-point instructions to perform computation on 256-bit vectors” [2, 5-28 Vol.1]. Therefore it can execute 2 (multiply-add) times 4 double-precision floating-point instructions each cycle. This results in 8 DP FLOPs per cycle.

Unfortunately no definite source could be found but according to Shimpi [4] the Haswell architecture has 2 FMA units, equalling to  $2 * 8 = 16$  DP FLOPs per core. This also aligns with information found on StackOverflow[1]. Furthermore there are 2 cores in a Core i5 processor. Taken together this results in  $16 * 2 = 32$  DP FLOPs per cycle for both cores.

At max frequency the processor is therefore capable of a theoretical peak performance of  $32 * 2.7 = 86.4$  GFLOP/s.

## References

- [1] Marat Dukhan. *FLOPS per cycle for sandy-bridge and haswell SSE2/AVX/AVX2*. URL: <http://stackoverflow.com/a/15657772> (visited on 06/20/2016).
- [2] Intel. *Intel® 64 and IA-32 Architectures Software Developer’s Manual. Combined Volumes: 1, 2A, 2B, 2C, 3A, 3B, 3C and 3D*. Intel. Apr. 2016. URL: <https://www-ssl.intel.com/content/dam/www/public/us/en/documents/manuals/64-ia-32-architectures-software-developer-manual-325462.pdf>.
- [3] Intel Ark. *Intel® Core™ i5-4210U Processor Specifications*. URL: <http://ark.intel.com/products/81016/> (visited on 06/19/2016).
- [4] Anand Lal Shimpi. *Haswell’s Wide Execution Engine*. Oct. 5, 2012. URL: <http://www.anandtech.com/show/6355/intels-haswell-architecture/8> (visited on 06/19/2016).

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<sup>1</sup>Fused Multiply Add

<sup>2</sup>Advanced Vector Extension

### 3 Kernels